IN THE CLAIMS

At the time the Office Action was mailed, claims 35, 37-39, 45, 47-49, 63 and 65-70 were pending. With this response, no amendments to the claims have been made. A listing of the claims and status indicators is provided below. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of the Claims

1-34. (Canceled)

35. (Previously presented) An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein each die in the stack of at least two semiconductor die is functional.

36. (Canceled)

37. (Previously presented) The integrated circuit, as set forth in claim 35, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

38. (Previously presented) An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

39. (Previously presented) The integrated circuit, as set forth in claim 35, wherein at least one of the at least two semiconductor die comprises a memory die.

40-44. (Canceled)

45. (Original) An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the

stack being coupled to a packaging substrate, wherein each die in the stack of at least two semiconductor die is functional.

46. (Canceled)

47. (Original) The integrated circuit, as set forth in claim 45, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

48. (Previously presented) An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate, wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

49. (Original) The integrated circuit, as set forth in claim 45, wherein at least one of the at least two semiconductor die comprises a memory die.

50-62. (Canceled)

63. (Previously presented) An integrate circuit package comprising:

a substrate; and

a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;

wherein each die in the stack of at least two semiconductor die is functional.

64. (Canceled)

65. (Previously presented) The integrated circuit package, as set forth in claim 63, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

66. (Previously presented) An integrate circuit package comprising:

a substrate; and

a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

67. (Previously presented) The integrated circuit package, as set forth in claim 63, wherein at least one of the at least two semiconductor die comprises a memory die.

68. (Previously presented) An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein each die in the stack of at least two die is successively thinner than the previous die.

69. (Previously presented) An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate, wherein each die in the stack of at least two semiconductor die is successively thinner than the previous die.

70. (Previously presented) An integrate circuit package comprising:

a substrate; and

a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;

wherein each die in the stack is successively thinner than the previous die.